



DC COMPONENTS CO., LTD.  
RECTIFIER SPECIALISTS

1N4148WS  
1N4448WS

TECHNICAL SPECIFICATIONS OF SURFACE MOUNT SWITCHING DIODE

VOLTAGE - 100 Volts

CURRENT - 0.15 Ampere

FEATURES

- \* Low power loss, high efficiency
- \* Low leakage
- \* Low forward voltage drop
- \* High speed switching
- \* High current capability
- \* High reliability

MECHANICAL DATA

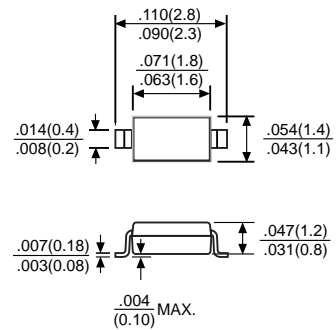
- \* Case: Molded plastic
- \* Epoxy: UL 94V-0 rate flame retardant
- \* Terminals: Solder plated, solderable per MIL-STD-202E, Method 208 guaranteed
- \* Mounting position: Any
- \* Weight: 0.008 grams Approx.

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified.  
Single phase, half wave, 60 Hz, resistive or inductive load.  
For capacitive load, derate current by 20%.



SOD-323



Dimensions in inches and (millimeters)

	SYMBOL	1N4148WS	1N4448WS	UNITS
Maximum DC Blocking Voltage	V <sub>DC</sub>		75	V
Maximum Recurrent Peak Reverse Voltage	V <sub>RRM</sub>		100	V
Maximum Average Rectified Current	I <sub>o</sub>		150	mA
Peak Forward Surge Current 8.3 ms single half sine-wave superimposed on rated load (JEDEC Method)	I <sub>FSM</sub>	2.0	4.0	A
Maximum Power Dissipation T <sub>amb</sub> =25°C	P <sub>tot</sub>		200	mW
Maximum Forward Voltage	V <sub>F</sub>	1.0 / 50mA	0.72 / 5mA 1.0 / 100mA	V
Maximum Reverse Current at Rated DC Blocking Voltage @ T <sub>A</sub> =25°C	I <sub>R</sub>		2.5	μA
Maximum Reverse Recovery Time(Note 1)	t <sub>rr</sub>		4.0	ns
Typical Junction Capacitance(Note 2)	C <sub>J</sub>		4.0	pF
Operating and Storage Temperature Range	T <sub>J</sub> ,T <sub>STG</sub>		-55 to + 125	°C

Note: 1. Test conditions: I<sub>F</sub>=I<sub>R</sub>=10mA, R<sub>L</sub>=100Ω, measured at I<sub>R</sub>=1mA  
2. Measured at 1MHz and V<sub>R</sub>=0

# RATING AND CHARACTERISTIC CURVES (1N4148WS AND 1N4448WS)

FIG.1 - TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

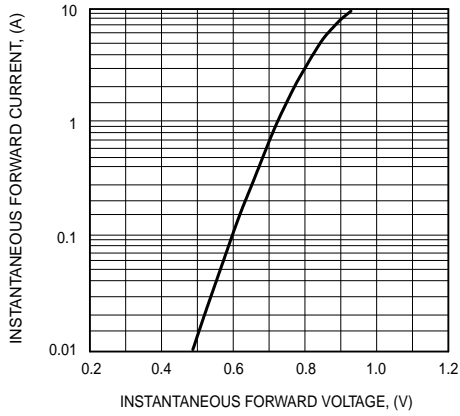


FIG.2 - TYPICAL REVERSE CHARACTERISTICS

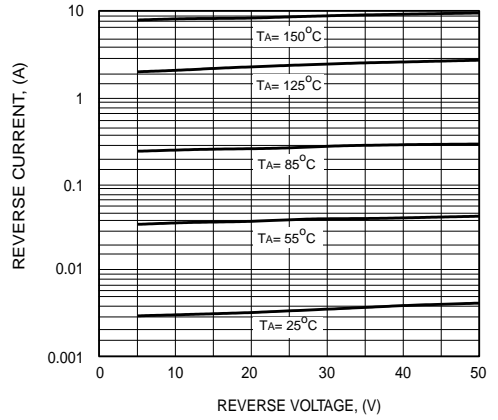


FIG.3 - TYPICAL JUNCTION CAPACITANCE

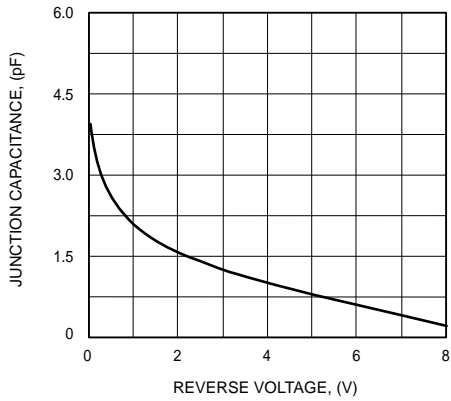


FIG.4 - RECTIFICATION EFFICIENCY MEASUREMENT CIRCUIT

